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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,683	04/20/2001	Robert L. Shuler JR.	MSC-22953-3	5289

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,683	SHULER, ROBERT L.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-16 and 22-37* is/are pending in the application.

4a) Of the above claim(s) *14-16 and 22-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13 and 30-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of the specie including Figures 6, 11A, 11B and 13 (note that applicant identify that claims 8-13 and 30-37 correspond to the above Figures) in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. The drawings are objected to because Figures 1 and 7A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: on line 21 of page 9, it appears that "2 =lambda" should be changed to --2*lambda--. Also, throughout the specification, the recitation "a gate" and "the gate" (where refers as a "logic gate") should be changed to --a logic gate-- and --the logic gate-- so that the disclosure is clear (i.e., to avoid a confusion with a gate terminal of a MOSFET transistor). Appropriate correction is required.

Claim Objections

4. Claims 8-13 and 30-37 are objected to because of the following informalities:

In claims 8-11, 30, 31 and 36, it is suggested that "gate" and "gates" in these claims be changed to --logic gate-- or --logic gates-- to avoid a confusion with gate of a MOSFET transistor.

In claim 8, line 2, "output;" should be changed to --output; and--.

In claim 8, line 4, "elements; and" should be changed to --elements; wherein--.

In claim 8, line 6, "input to the" should be changed to --input of the--.

In claim 31, line 3, "wherein providing" should be changed to --wherein said providing step--.

In claim 31, line 4, "a delay into" should be changed to --a delay circuit into--.

In claim 32, line 1, "wherein adjusting" should be changed to --wherein said adjusting step--.

In claim 33, line 1, "wherein increasing" should be changed to --wherein said increasing step--.

In claim 34, line 1, "wherein making" should be changed to --wherein said making step--.

Appropriate correction to the above informalities is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 8-13 and 30-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 8, "a standard glitch" is indefinite because it is unclear what type of glitch is a standard glitch or a non-standard glitch. Further, "the delay" on line 7 is unclear antecedent basis and it is not clear the delay of what (i.e., delay of the SEU-resistance circuit or what). Note that "the delay" on line 1 of claim 9 is indefinite for the similar problem.

Claims 9-13 are indefinite because they include the indefinite problem of claim 8.

In claim 10, the recitation "wherein the delay elements comprise balanced gates" is indefinite because it is not clear what a "balanced gate" is. Note that, line 26 of page 7 of the specification recites that Figure 7B is a balanced gate; and it is seen that the circuit in Figure 7B is a 4 inputs logic NAND gate. However, the disclosure discloses that the delay circuit (Figure 2) that is used in the latch (602, Figure 6) comprises inverters. Thus, the recitation "balance gates" recited in claim 10 is indefinite because it is not clear what exactly applicant means, and what logic gate is considered to be "balanced gate".

In claim 30, "providing a delay in the gate" is indefinite because it is not clear what it means exactly (i.e., does it mean that the logic gate having a delay). Clarification is requested.

Claims 32-37 are indefinite because they include the indefinite problem of claim 31.

In claims 31 and 32, it appears that the recitation "adjusting the characteristics of the channel of the channel of the first FET, the characteristics of the channel of the second FET and the parasitic capacitance of the node" on line 5-7 of claim 31, and "increasing the length of the channel of the first FET" on line 2 of claim 32 are misdescriptive because it is inconsistent with

what is disclosed in the specification. It is seen that the latch recites in this claim is shown in Figure 6, the delay circuit is circuit 602 (Figure 6), and the gate is circuit 612 (Figure 6, which includes first FET M5 and second FET M8 wherein the gate terminal of the transistors M5 and M8 are connected together). The disclosure does not specifically disclose the providing a delay in the gate circuit by adjusting the characteristics of the channel of the first and second FETs (M5 and M8, Figure 6), or increasing the length of either channel of the first and second FETs. Note that the disclosure discloses on page 10, lines 18-27 (Figures 5A-5B) about the increasing the length of a field effect transistor to produce the results shown in Figure 4 (filter out glitches). However, the discussion as disclosed on lines 18-27 of page 10 (Figure 5A-5B) is for the delay circuit of Figure 2 (see lines 21-22 of page 7 of the instant specification), i.e., it is not discussed for the increasing the length (or adjusting the channel characteristics) of the FETs of the gate circuit in the latch. Clarification and/or appropriate correction is requested.

Claims 33-36 are indefinite because they include the indefinite problems of claims 31 and/or 32 as discussed above.

Also in claims 33 and 34, "the channel" is indefinite because it is not clear whether it refers to the channel of the first FET, or the channel of the second FET.

In claim 37, "the time constant" and "the threshold" on line 2 lack antecedent basis. Further, it is not understood the "time constant" of what, and the "threshold" of what. Further, it is not understood what is "L3" in this claim. Further, "would" on lines 5 and 9 is not a positive recitation of the invention, and therefore needs to be deleted. Further, "the threshold device" on line 6 lacks antecedent basis. Further, it is not clear what "length approximately L5" is (i.e., length approximately equals to L5 or what). Further, "a delay" on lines 7 and 11 are unclear

antecedent basis because it is not clear whether it is the same as the "delay" recited on line 5 of independent claim 30. Thus, claim 37 contains too many indefinite problems as discussed, and thus, this claim is unclear and is not understood.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 8-13 and 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Bansal (USP 5,504,703).

With respect to claim 8, Figure 3 of the Bansal reference discloses a latch circuit, which includes: a logic gate (T1, T2) having an input (node 4) and an output (node 1); and a feedback path (path goes from node 1 to node 4) from the output (node 1) to the input (node 4) of the logic gate, wherein the feedback path includes two or more delay elements (INV1, INV2, INV3, INV4); wherein the logic gate and the two or mode delay elements are configured to absorb a glitch at the input of the logic gate before it propagates through the feedback path to the input of the logic gate (Col. 3, lines 28-36 and 52-64), and the delay being spread among the gate and the two or more delay elements (inherent because every logic element must have a delay therein, so the delay spread among the elements in the latch circuit).

Note with claim 9, because every element in the latch is an inverter, and because reference does not specifically state the delay of each inverters in the latch is different, so it is

reasonable to construe that the delay being spread evenly among the logic gate and the inverters in the feedback path.

Note with claim 10, because delay elements in Figure 3 are inverters as applicant invention, so it is reasonable to construe that the delay elements comprise balance gates.

Note with claim 11, the feedback path includes a driver gate (T3, T4).

Now with claims 12 and 13, the delay elements (INV1, INV2, INV3, INV4) comprises inverters and the number of inverters is even.

With respect to claims 30-31 and 36, Figure 3 of the Bansal reference discloses a latch circuit which includes all the structure limitations as discussed in claims 8-13 above, so it also deem to meet all the method steps recited in claims 30 and 31. Note that it is seen in Figure 3 that the logic gate (T1, T2) having a first FET (T1) and a second FET (T2) each having a channel (gate of the transistor) connected at a node (node 4) having a parasitic capacitance (inherent because every transistor must have a parasitic capacitance between its gate to its source/drain/body), and the feedback path controlling the node 4 so the characteristics of the channel of the FETs (T1, T2) and the parasitic capacitance at node 4 must be adjusting/controlling. Note that the threshold device is the inverter T3-T4 in Figure 3 of Bansal which is coupled to the output (node 1) of the logic gate (T1-T2, by way of delay inverters INV1-INV2), and the threshold device having a threshold (inherent, i.e., the level at which the output of the inverter is changed to H when the input of the inverter is less than the threshold, and changed to L when the input of the inverter is greater than the threshold).

Conclusion

9. Note with claims 32-35 and 37, in view of the significant indefiniteness problems noted above, no prior art can be applied against these claims at this time. This is not an indication of allowability to these claims.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

March 11, 2004
Lnguyen

Long Nguyen
Art Unit: 2816